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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,361	04/29/2004	Eric A. Foreman	BUR920040075US1	3360

29625 7590 12/23/2005

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EXAMINER	
LE, TOAN M	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/709,361	FOREMAN ET AL.
	Examiner	Art Unit
	Toan M. Le	2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-22* is/are allowed.

6)☒ Claim(s) *1,2,9,10,12,23,24,26 and 28-34* is/are rejected.

7)☒ Claim(s) *3-8,11,25 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 31 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 12. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 9-10, 12, 23-24, 26, and 28-34 are rejected under 35 U.S.C. 102(b) as being "A General Probabilistic Framework for Worst Case Timing Analysis" by Orshansky et al. (referred hereafter Orshansky et al.).

Referring to claims 1, 12, and 31, Orshansky et al. disclose a method and a computer-readable medium containing instructions thereon that, when executed, cause a computer analyzing timing in an integrated circuit (Abstract), comprising:

identifying at least one set of racing paths within the integrated circuit, the at least one set of racing paths including an early path and a late path (page 557, 2nd col., section 4.2: 1st paragraph; equations 1-2);

identifying at least one delay characteristic of one or more elements in the early path and at least one delay characteristic of one or more elements in the late path (page 558, 1st col., lines 3-16);

grouping ones of the one or more elements in the early path with ones of the one or more elements in the late path having similar delay characteristics (page 557, 2nd col., section 4.2: 2nd and 3rd paragraph; page 558, 1st col., 2nd paragraph; equations 3-5); and

deriving an adjusted timing slack for the at least one set of racing paths by at least partially canceling delay contributions from grouped elements having similar delay characteristics (page 558, 1st col., lines 17-29; equations 4-5).

As to claim 2, Orshansky et al. disclose a method of analyzing timing in an integrated circuit (Abstract), wherein the similar delay characteristics comprise correlated delay functions (page 558, 1st col., lines 17-29; equations 4-5).

Referring to claim 9, Orshansky et al. disclose a method of analyzing timing in an integrated circuit (Abstract), wherein the similar delay characteristics comprise location-based delay characteristics (page 557, section 4.1; page 560, 2nd col., section 6: 1st paragraph).

As to claim 10, Orshansky et al. disclose a method of analyzing timing in an integrated circuit (Abstract), wherein the grouped elements comprise one or more pairs of elements, one element of each of the one or more pairs from the early path and one element of each of the one or more pairs from the late path (page 560, 2nd col., section 6: 1st paragraph; Table 2).

Referring to claims 23 and 30, Orshansky et al. disclose a method and a computer-readable medium containing instructions thereon that, when executed, cause a computer analyzing timing in an integrated circuit (Abstract), comprising:

identifying a late path to a timing test and an early path to a timing test (page 557, 2nd col., section 4.2: 1st paragraph; equations 1-2);

determining by using location information at least one pair of one element of the late path and one element of the early path (page 557, section 4.1; page 560, 2nd col., section 6: 1st paragraph);

computing by using the location information a variation in a difference in delays of the elements of the at least one pair (page 560, 2nd col., section 6: 1st and 2nd paragraphs; Table 2); and

deriving from the variation a slack for the late path to the timing test and the early path to the timing test (Table 2).

As to claim 24, Orshansky et al. disclose a method of analyzing timing in an integrated circuit (Abstract), wherein the at least one pair comprises several pairs (Table 2).

Referring to claim 26, Orshansky et al. disclose a method of integrated circuit (Abstract), wherein the location infor mation comprises physical location coordinates (Table 2).

As to claims 28-29, Orshansky et al. disclose a method of analyzing timing in an integrated circuit (Abstract), wherein the integrated circuit is an existing/newly integrated circuit (Table 2).

Referring to claims 32-34, Orshansky et al. disclose a method of analyzing timing in an integrated circuit (Abstract), further comprising, prior to the deriving, generating an exposure report containing information on a timing slack for each identified set of racing paths and adjustments that can be made to the timing slack (page 558, 1st col., lines 30-37).

Allowable Subject Matter

Claims 3-8, 11, 25, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of the claims 3-5 is the inclusion of summing delay contributions of ungrouped elements in the early/late path, calculating a delay difference between the early path and late path by using the summed delay contributions of the ungrouped elements in the early/late paths, and subtracting the delay difference from the initial timing slack, wherein the summing comprises root sum squaring and root sum square difference.

The reason for allowance of the claims 6-8 is the inclusion of calculating metal layer delays for the early and late paths, summing like metal layer delay contributions in the early/late paths, calculating a metal layer delay difference between the metal layer delay contributions for the early path and late path, and subtracting the metal layer delay difference from the initial timing slack, wherein the summing comprises root sum squaring and root sum square difference.

The reason for allowance of the claim 11 is the inclusion of computing a variation in a difference in delays of the one or more pairs of elements by using the location-based delay characteristics and subtracting the variation from an initial timing slack.

The reason for allowance of the claim 25 is the inclusion of adding the variation of unpaired elements to the slack.

The reason for allowance of the claim 27 is the inclusion of identifying one or more failing tests of the static timing analysis and using an early path/late path of one or more failing tests as the early path/late path of the timing tests.

Allowable Subject Matter

Claims 13-22 are allowed.

The reason for allowance of the claims 13-22 is the inclusion of sorting the delay contributions into groups with similar delay contributions including groups of correlated delay contributions and groups with dissimilar delay contributions, canceling the delay contributions of the groups with similar delay contributions, and comparing the delay contributions of the groups with dissimilar delay contributions with an initial timing slack calculated for the set of racing paths, wherein the delay contributions comprise cell-based/wire-dependent and cell-based and wire-dependent delay contributions of the existing/newly-designed integrated circuit including performing a static timing analysis to identify a failing test of the static timing analysis in order to use a set of racing paths of the failing test.

Response to Arguments

Applicant's arguments filed 10/14/05 have been fully considered but they are not persuasive.

Referring to claims 1 and 31, Applicant argues that "However, it is not apparent that Orshansky discloses, or even suggests, grouping ones of the one or more elements in the early path with ones of the one or more elements in the late path having similar delay characteristics and/or deriving an adjusted timing slack for the at least one set of racing paths by at least partially canceling delay contributions from grouped elements having similar delay characteristics."

Orshansky discloses "The cumulative probability function of $\max\{D_1 \ldots D_N\}$ is given by $F(t) = P\{\max\{D_1 \ldots D_N\} \leq t\}$, or equivalent: $F(t) = P\{D_1 \leq t, D_2 \leq t, \ldots, D_N \leq t\}$ where F(t) is the cumulative probability function defined over the path delay probability space. In general, we can

find the cumulative probability function by direct integration: $F(t) = \int(N\text{-}1) \int f(D_1, D_2, \ldots D_N)$ $dD_1 dD_2 \ldots dD_N$ where $f(D_1, D_2, \ldots D_N)$ is the joint probability density function (jpdf) of (D_1, $D_2, \ldots D_N$) on page 557, section 4.1.

Thus, Orshansky does disclose grouping ones of the one or more elements in the early path (cumulative probability function) with ones of the one or more elements in the late path (joint probability density function) having similar delay characteristics.

In addition, Orshansky discloses "Let the delay of a gate be given by an arbitrary function $d_g = f(L)$. In order to establish an expression for the pair-wise covariances of gate delay, we assume the linearity of delay response to the localized variation of process parameters. In other words, we assume that a first order Taylor expansion of the gate delay function is adequate. Then, $d_g = d_g(L_o) + \varphi(L_o)^T M$" on page 558, 1st col., lines 17-23.

Thus, Orshansky does disclose deriving an adjusted timing slack for the at least one set of racing paths by at least partially canceling delay contributions from grouped elements having similar delay characteristics.

As to claim 23, Applicant argues that "Moreover, while the Examiner has alleged that tables 2 and 3 of Orshansky discloses computing, by using the location information, a variation in a difference in delays of the elements of the at least one pair and deriving from the variation a slack for the late path to the timing test and the early path to the timing test, the Examiner has failed to identify any specific language in this document in support of such assertions."

Orshansky discloses "We now consider a simple circuit example that will illustrate several features of the probabilistic framework for worst-case timing analysis proposed in the previous sections. To highlight the important features of the approach, we constructed a

topologically simple circuit that consists of a repeated pattern of 4 uniquely constructed paths. The four unique paths have similar but non-identical mean delays, E(D). Because paths contain different number and types of cells, the variance of path delays, σ^2_D, is also different. (This way, path 4 whose $E(D_4) < E(D_1)$ may be stochastically slower than path 1, because $\sigma_4 > \sigma_1$.) on page 560, 2nd col., section 6: 1st paragraph.

Thus, Orshansky does disclose computing, by using the location information, a variation in a difference in delays of the elements of the at least one pair and deriving from the variation a slack for the late path to the timing test and the early path to the timing test.

Conclusion

THIS ACTION IS MADE FINAL.

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

December 20, 2005

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